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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,299	11/27/2001	Woon-kyung Lee	4591-222	9003

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EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,299	LEE, WOON-KYUNG	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *2 and 3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1&4-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 1, 4-6 and 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kume et al., (US 5,188,976).

In re claims 1, 4-6 and 9-13, Kume et al, in related text (Col. 7, Lines 13-39) and figures (Figs. 3A-3E) disclose a method of fabricating a flash memory device having a cell array region and a peripheral circuit region, the method comprising: forming a device isolation layer 2 at a predetermined region of a semiconductor substrate 1 to define at least one first active region in the cell array region and a second active region in the peripheral circuit region; forming a floating gate pattern 5 covering the first active region and a gate conductive layer 5 covering the peripheral circuit region; forming a tunnel oxide layer 4 interposed between the floating gate pattern 5 and the first active region; forming a gate oxide layer 4 interposed between the gate conductive layer 5 and the second active region; implanting impurity ions into the first and

second active regions prior to formation of the tunnel oxide layer and the gate oxide layer (Col. 9, Lines 53-63; Col. 12, Lines 41-47); sequentially forming an inter-gate dielectric layer 6 and a control gate conductive layer 7 on an entire surface of the substrate 1 having the floating gate pattern 5 and the gate conductive layer 5; and selectively removing the control gate conductive layer 7 and the inter-gate dielectric layer 6 which are located in the peripheral circuit region, thereby exposing the gate conductive layer 5 in the peripheral circuit region; forming a metal silicide layer 10a on the control gate conductive layer 7 in the cell array region and the exposed gate conductive layer 5 in the peripheral circuit region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-6 and 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (US 2002/0008278A1) in view of Lee et al. (US 5,292,681).

In re claims 1 and 12, Mori, in related text ([0138]) and figures (Figs. 14A-14D) discloses a method of fabricating a flash memory device having a cell array region and a peripheral circuit region, the method comprising: forming a device isolation layer 14 at a predetermined region of a semiconductor substrate10 to define at least one first active region in the cell array region and a

second active region in the peripheral circuit region; forming a floating gate pattern 22/24 covering the first active region and a gate conductive layer 22/24 covering the peripheral circuit region; forming a tunnel oxide layer 21a interposed between the floating gate pattern and the first active region; forming a gate oxide layer 21b interposed between the gate conductive layer and the second active region; implanting impurity ions into the first and second active regions (See [0123]-[0124] and Fig. 1); sequentially forming an inter-gate dielectric layer 26 and a control gate conductive layer 28 on an entire surface of the substrate 10 having the floating gate pattern 22/24 and the gate conductive layer 22/24; and selectively removing the control gate conductive layer 28 and the inter-gate dielectric layer 26 which are located in the peripheral circuit region, thereby exposing the gate conductive layer 24 in the peripheral circuit region.

Mori discloses all claimed subject matter, but fails to expressly discloses the step of implanting impurity ions prior to formation of the gate oxide layer and tunnel oxide layer.

Lee et al., in figures (Figs. 19-21 and 25-26) disclose the feature of implanting impurity ions into the cell array region and peripheral circuit region to form a well prior to formation of the gate oxide layer and tunnel oxide layer. Therefore, it would have been an obvious to an ordinary skill in the art at the time of the invention to apply the method steps as taught by Lee et al. on the method of Mori. In order to form a well and to adjust a threshold voltage of a MOS transistor, implanting impurity ions into the active region is generally used. It will be apparent to those skilled in the art that various modifications, improvements, combinations, and the like can be made.

In re claims 4-6, in which the floating gate pattern and the gate conductive layer are formed of a doped polysilicon layer by ion implantation, using one of phosphor ion and arsenic ion as dopants (See [0130]; [0006]; [0010] and [0148])

In re claim 8, in which forming the device isolation layer, the floating gate pattern and the gate conductive layer includes: forming a lower conductive layer on the entire surface of the semiconductor substrate; sequentially patterning the lower conductive layer and the semiconductor to form a trench region at a predetermined region of the semiconductor substrate and concurrently define at least one first active region in the cell array region and a second active region in the peripheral circuit region (See [0128]–[0129] and Fig. 6); forming a device isolation layer filling the trench region; forming an upper conductive layer on the entire surface of the substrate having the device isolation layer; and patterning the upper conductive layer to form a floating gate pattern covering the first active region and a gate conductive layer covering the peripheral circuit region, the floating gate pattern and the gate conductive layer being composed of a portion of the lower conductive layer and a portion of the upper conductive layer (See [0146] and Figs. 14A-D)

In re claims 9-10 and 13, further comprising: forming a metal silicide layer 29 on the control gate conductive layer 28 in the cell array region and the exposed gate conductive layer 24 in the peripheral circuit region (See [0145] and Fig. 14D)

In re claim 11, further comprising: patterning the control gate conductive layer, the inter-gate dielectric layer and the floating gate pattern that are located in the cell array region, thereby forming a word line crossing over the first active region and a floating gate interposed between the word line and the first active region; and patterning the gate conductive layer that are located

in the peripheral circuit region, thereby forming a gate electrode crossing over the second active region. (See [0145] and Figs. 14A-14D).

In re claim 14, wherein forming the tunnel oxide layer 21a/21c and forming the gate oxide layer 21b comprises forming the gate oxide layer 21b to a thickness different from that of the tunnel oxide layer 21a/21c (See [0125] and Fig. 14D).

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (US 2002/0008278A1) in view of Hayakawa (US 5,976,934).

Mori discloses all claimed subject matter, but fails to expressly discloses the doped polysilicon layer is formed using $POCl_3$.

Hayakawa, in related text, (Col. 10, Lines 1-15) discloses the doped polysilicon layer is formed using $POCl_3$ as a dopant source. It would have been obvious to one of ordinary skill in the art at the time the invention was made by using $POCl_3$ as a dopant source of Hayakawa for reduce the resistance of the polysilicon layer, within the general skill of a worker in the art, to select a known material on the basis of its suitability for its intended use is a matter of obvious design choice.

Response to Arguments

4. Applicant's arguments filed 05/19/04 have been fully considered but they are not persuasive.

It is argued, at page 5 of the remarks, that Kume '976 fails to anticipate the present invention because "Kume does not teach the recited feature of implanting impurity ions into the first and second active regions to adjust a threshold voltage of a MOS transistor....". Note that Kume clearly teaches implanting impurity ions into the first and second active regions prior to formation of the tunnel oxide layer and the gate oxide layer (Col. 9, Lines 53-63; Col. 12, Lines 41-47). It will be apparent to those skilled in the art that using ion implantation step to adjust the threshold voltage in the active areas is a well known techniques (See prior art reference **USPAT 4,163,985**{Col. 3, Lines. 60-65} for evidence of the state of the art in which a surface area of the substrate is subjected to the ion implantation of boron ions in order to adjust the threshold voltage of the MOS transistor).

In response to Applicant's argument on page 7 that "...Lee is teaching the use of diffusion process rather than an ion implantation process. "Diffusion" is the common name for a high temperature doping process during which dopant atom (not ions) are introduced into a semiconductor by diffusion of the dopant atoms"....". Lee, in related text (Col. 8, line 36 and 64-65) discloses that the p-well is a P-well implant and n-well is a phousphorus implant.

Therefore, the rejection of claims 1 and 4-14, as stated in the previous Office Action is maintained.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action

is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is 571-272-1798. The examiner can normally be reached on Monday-Friday 8:00am-5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

David Vu.

David Nelms
Supervisory Patent Examiner
Technology Center 2800